What is claimed is:

Sub a2 1. A multiple-format video encoder for encoding digital RGB signals in a plurality of video formats, comprising:

a color-difference signal generating circuit for generating a color-difference signal from the RGB signals;

a memory for storing values of trigonometric functions covering a predetermined number of cycles at addresses corresponding to evenly spaced phases;

an address calculating circuit for calculating addresses at which to access the memory in accordance with the video format actually used; and

a multiplying circuit for multiplying the color-difference signal by values calculated from the values of the trigonometric functions stored at the addresses specified by the address calculating circuit.

2. A multiple-format video encoder as claimed in claim 1,

wherein the address calculating circuit comprises:

a value selecting circuit for selecting a predetermined value to be added in accordance with the video format actually used;

an adder for adding the value to be added selected by the value selecting circuit to the addresses specified by the address calculating circuit; and

a flip-flop circuit for temporarily storing values output from the adder and refreshing those values in synchronism with regular clock pulses so that the addresses are refreshed with those values.

3. A multiple-format video encoder as claimed in claim 2,

wherein the address calculating circuit comprises a shift circuit for dividing the addresses output from the flip-flop circuit by a shift operation to obtain addresses at which to access the memory.

4. A multiple-format video encoder as claimed in claim 1,

wherein the color-difference signal includes color-difference signals B-Y and R-Y,

wherein the values of the trigonometric functions include values of sine and cosine functions, and

wherein the multiplying circuit comprises:

a first multiplying circuit for multiplying the color-difference signal B-Y by the values of the sine function;

a second multiplying circuit for multiplying the color-difference signal R-Y by values calculated from the values of the cosine function; and

an adding circuit for adding an output of the first multiplying circuit to an output of the second multiplying circuit to obtain a carrier chrominance signal.

5. A multiple-format video encoder as claimed in claim 4, further comprising:

an inverting circuit for inverting polarity of the values of the cosine

function; and

a switch for feeding the second multiplying circuit alternately with the values of the cosine function intact, for one scanning line of the RGB signals, and with the values of the cosine function after inversion by the inverting circuit, for a next line of the RGB signals, and so forth.

6. A multiple-format video encoder as claimed in claim 5,

wherein the video format used include an NTSC format and a PAL format, and

wherein, when the NTSC format is used, the switch keeps feeding the second multiplying circuit with the values of the cosine function intact, and, when the PAL format is used, the switch feeds the second multiplying circuit alternately with the values of the cosine function intact, for one scanning line of the RGB signals, and with the values of the cosine function after inversion by the inverting circuit, for a next line of the RGB signals, and so forth.

7. A multiple-format video encoder as claimed in claim 4,

wherein the value to be added has a different value depending on whether an NTSC, PAL, PAL-M, or PAL-N format is used.

8. A multiple-format video encoder as claimed in claim 4, further comprising:

a luminance signal generating circuit for generating a luminance signal from the RGB signals.

9. A multiple-format video encoder as claimed in claim 8, further comprising:

an adding circuit for adding the luminance signal to the carrier chrominance signal to obtain a video signal.

10. A multiple-format video encoder as claimed in claim 8,

wherein the memory is so mapped that one cycle is covered by a total of 1024 values of the trigonometric functions that are addressed individually with 10-bit addresses, and the value to be added and the addresses output from the flip-flop circuit are 20-bit values, the shift circuit dividing those 20-bit addresses by 1024 to obtain the 10-bit addresses.

11. An electronic appliance having a multiple-format video encoder that encodes digital RGB signals in a plurality of video formats,

wherein the multiple-format video encoder comprises:

a color-difference signal generating circuit for generating a color-difference signal from the RGB signals;

a memory for storing values of trigonometric functions covering a predetermined number of cycles at addresses corresponding to evenly spaced phases;

an address calculating circuit for calculating addresses at which to access the memory in accordance with the video format actually used; and

a multiplying circuit for multiplying the color-difference signal by values calculated from the values of the trigonometric functions stored at the addresses specified by the address calculating circuit.

12. An electronic appliance as claimed in claim 11,

wherein the address calculating circuit comprises:

a value selecting circuit for selecting a predetermined value to be added in accordance with the video format actually used;

an adder for adding the value to be added selected by the value selecting circuit to the addresses specified by the address calculating circuit; and

a flip-flop circuit for temporarily storing values output from the adder and refreshing those values in synchronism with regular clock pulses so that the addresses are refreshed with those values.